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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/603,734	06/24/2003	Eric R. Keller	X-1281 US	3289

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EXAMINER	
LEVIN, NAUM B	

ART UNIT	PAPER NUMBER
2825	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/603,734	KELLER ET AL.	
	Examiner	Art Unit	
	Naum B. Levin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 April 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) *18-21* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17 and 22-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/24/3,6/24/5.1/30/7*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/603,734 and Response to election/restriction filed on 4/12/2007. Applicant has provisionally elected claims 1-17 and 22-31 (Group 1) with traverse. Claims 18-21 (Group 2) are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected. Applicant timely traversed the restriction (election) requirement in the reply filed on 4/12/2007.

2. The possible inventions of Group 1 (claims 1-17 and 22-31) and Group 2 (claims 18-21) related to a method of implementing a design in a PLD to reduce susceptibility to single-event upsets, but Group 2 includes additional utility, such as: "**performing post-processing of the routed design**".

Applicant's Specification also distinguishes these groups as: "**In some embodiments, the duplicate paths are provided during the routing phase** of the place-and-route implementation of the PLD design. **In other embodiments, a post-processing step performed** on a previously placed and routed PLD design adds additional paths to reduce the susceptibility of the design to SEUs – [0014]".

As such, the restriction is hereby made final.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1- 17 and 22-31 are rejected under 35 U.S.C. 102(b) as being anticipated by de Lima ("Designing single event upset mitigation techniques for large SRAM-based FPGA devices"; Thesis Proposal; Porto Alegre, February 11th, 2002).

4. As to claims 1, 8, 10, 12, 20, 22, 28 and 30 de Lima discloses:

(1) A method of implementing a design in a programmable logic device (PLD) to reduce susceptibility to single-event upsets (SEUs), the design comprising source logic, destination logic, and a node coupled between the source logic and the destination logic, the method comprising (page 7):

assigning (The architecture of a programmable device is based on an array of logic blocks that can be programmable by the interconnections to implement different designs – page 16; The CLBs are interconnected through a general routing matrix (GRM) that comprises an array of routing switches located at the intersections of horizontal and vertical routing channels – page 28) the source logic to a first logic block in the PLD (Some hex wires can only drive data out of the CLB; these are called unidirectional out – page 30) (pages 16, 28, 30, 33, 39-41);

assigning the destination logic to a second logic block in the PLD (Some hex wires can only drive data into the CLB – page 30) (pages 16, 28, 30, 33, 39-41);

identifying first and second data input terminals of a programmable routing multiplexer in the PLD (A voter (or majority circuit) is implemented by the top MUX to create a "hardened" output ... terminals D, G – fig.2.6, page 18), wherein a selection between the first and second data input terminals is determined by a first value stored in

a first memory cell controlling the programmable routing multiplexer (If both A and B read logic zero, MUX input D0 is selected – page 18) (pages 18, 25, 53- 54);

routing the node on a first routing path between the first and second logic blocks, wherein the first routing path traverses the programmable routing multiplexer via the first data input terminal (If A and B disagree due to an SEU (or for other reasons), the MUX will select flip-flop C. We know C agrees with either A or B, and thus the MUX "voted" to produce data agreed on by two of the three flip-flops – page 18); and

routing the node on a second routing path between the first and second logic blocks, wherein the second routing path traverses the programmable routing multiplexer via the second data input terminal (If A and B disagree due to an SEU (or for other reasons), the MUX will select flip-flop C. We know C agrees with either A or B, and thus the MUX "voted" to produce data agreed on by two of the three flip-flops – page 18).

(8) A computer-readable storage medium comprising computer-executable code for implementing a design in a programmable logic device (PLD) to reduce susceptibility to single-event upsets (SEUs), the design comprising source logic, destination logic, and a node coupled between the source logic and the destination logic, the medium comprising (pages 7, 43):

assigning (The architecture of a programmable device is based on an array of logic blocks that can be programmable by the interconnections to implement different designs – page 16; The CLBs are interconnected through a general routing matrix (GRM) that comprises an array of routing switches located at the intersections of horizontal and vertical routing channels – page 28) the source logic to a first logic block

in the PLD (Some hex wires can only drive data out of the CLB; these are called unidirectional out – page 30) (pages 16, 28, 30, 33, 39-41);

assigning the destination logic to a second logic block in the PLD (Some hex wires can only drive data into the CLB – page 30) (pages 16, 28, 30, 33, 39-41);

identifying first and second data input terminals of a programmable routing multiplexer in the PLD (A voter (or majority circuit) is implemented by the top MUX to create a "hardened" output ... terminals D, G – fig.2.6, page 18), wherein a selection between the first and second data input terminals is determined by a first value stored in a first memory cell controlling the programmable routing multiplexer (If both A and B read logic zero, MUX input D0 is selected – page 18) (pages 18, 25, 53- 54);

routing the node on a first routing path between the first and second logic blocks, wherein the first routing path traverses the programmable routing multiplexer via the first data input terminal (If A and B disagree due to an SEU (or for other reasons), the MUX will select flip-flop C. We know C agrees with either A or B, and thus the MUX "voted" to produce data agreed on by two of the three flip-flops – page 18); and

routing the node on a second routing path between the first and second logic blocks, wherein the second routing path traverses the programmable routing multiplexer via the second data input terminal (If A and B disagree due to an SEU (or for other reasons), the MUX will select flip-flop C. We know C agrees with either A or B, and thus the MUX "voted" to produce data agreed on by two of the three flip-flops – page 18);

(10) A computer system for implementing a design in a programmable logic device (PLD) to reduce susceptibility to single-event upsets (SEUs), the design

comprising source logic, destination logic, and a node coupled between the source logic and the destination logic, the computer system comprising (pages 7, 43):

assigning (The architecture of a programmable device is based on an array of logic blocks that can be programmable by the interconnections to implement different designs – page 16; The CLBs are interconnected through a general routing matrix (GRM) that comprises an array of routing switches located at the intersections of horizontal and vertical routing channels – page 28) the source logic to a first logic block in the PLD (Some hex wires can only drive data out of the CLB; these are called unidirectional out – page 30) (pages 16, 28, 30, 33, 39-41);

assigning the destination logic to a second logic block in the PLD (Some hex wires can only drive data into the CLB – page 30) (pages 16, 28, 30, 33, 39-41);

identifying first and second data input terminals of a programmable routing multiplexer in the PLD (A voter (or majority circuit) is implemented by the top MUX to create a "hardened" output ... terminals D, G – fig.2.6, page 18), wherein a selection between the first and second data input terminals is determined by a first value stored in a first memory cell controlling the programmable routing multiplexer (If both A and B read logic zero, MUX input D0 is selected – page 18) (pages 18, 25, 53- 54);

routing the node on a first routing path between the first and second logic blocks, wherein the first routing path traverses the programmable routing multiplexer via the first data input terminal (If A and B disagree due to an SEU (or for other reasons), the MUX will select flip-flop C. We know C agrees with either A or B, and thus the MUX "voted" to produce data agreed on by two of the three flip-flops – page 18); and

routing the node on a second routing path between the first and second logic blocks, wherein the second routing path traverses the programmable routing multiplexer via the second data input terminal (If A and B disagree due to an SEU (or for other reasons), the MUX will select flip-flop C. We know C agrees with either A or B, and thus the MUX "voted" to produce data agreed on by two of the three flip-flops – page 18);

(12) A method of implementing a design in a programmable logic device (PLD) to reduce susceptibility to single-event upsets (SEUs), the design comprising source logic, destination logic, and a node coupled between the source logic and the destination logic, the method comprising (page 7):

generating a PLD placement wherein the source logic is assigned to a first logic block in the PLD and the destination logic is assigned to a second logic block in the PLD (pages 14-16, 28, 30, 33, 39-42, 47);

routing the PLD placement to generate a routed design wherein the node is routed on a first routing path between the first and second logic blocks, the first routing path traversing a programmable routing multiplexer via a first data input terminal of the programmable routing multiplexer (page 18);

identifying a second data input terminal of the programmable routing multiplexer, wherein a selection between the first and second data input terminals is determined by a first value stored in a first memory cell controlling the programmable routing multiplexer (pages 18, 25, 53- 54); and

routing the node on a second routing path between the first and second logic blocks, wherein the second routing path traverses the programmable routing multiplexer via the second data input terminal (page 18);

(22) A method of implementing a design in a programmable logic device (PLD) to reduce susceptibility to single-event upsets (SEUs), the method comprising (page 7):

identifying in a programmable routing multiplexer of the PLD a first data input terminal and a second data input terminal, wherein a selection between the first and second data input terminals is determined by a first value stored in a first memory cell controlling the programmable routing multiplexer (pages 18, 25, 53- 54);

routing a node in the design to the first data input terminal (page 18); and

routing the node to the second data input terminal (page 18);

(28) A computer-readable storage medium comprising computer-executable code for implementing a design in a programmable logic device (PLD) to reduce susceptibility to single-event upsets (SEUs), the medium comprising (pages 7, 43):

identifying in a programmable routing multiplexer of the PLD a first data input terminal and a second data input terminal, wherein a selection between the first and second data input terminals is determined by a first value stored in a first memory cell controlling the programmable routing multiplexer (pages 18, 25, 53- 54);

routing a node in the design to the first data input terminal (page 18); and

routing the node to the second data input terminal (page 18);

(30) A computer system for implementing a design in a programmable logic device (PLD) to reduce susceptibility to single-event upsets (SEUs), the computer system comprising (pages 7, 43):

identifying in a programmable routing multiplexer of the PLD a first data input terminal and a second data input terminal, wherein a selection between the first and second data input terminals is determined by a first value stored in a first memory cell controlling the programmable routing multiplexer (pages 18, 25, 53- 54);

routing a node in the design to the first data input terminal (page 18); and

routing the node to the second data input terminal (page 18).

5. As to claims 2-7, 9, 11, 13-17, 21, 23-27, 29 and 31 de Lima recites:

(2), (13), (23) The method further comprising identifying a third data input terminal of the programmable routing multiplexer (pages 19-20);

(3), (14), (24) The method, wherein the PLD is a field programmable gate array (FPGA) (page 16);

(4), (15), (25) The method, wherein the first memory cell is a static RAM-based configuration memory cell of the FPGA (page 17);

(5), (16), (26) The method, wherein the multiplexer is a 4-to-1 multiplexer (pages 28-29, 33);

(6) The method, wherein the identifying and the routing are performed interactively with each other (pages 18, 25, 53- 54);

(7), (9), (11), (17), (27), (29), (31) The method/program/system further comprising evaluating the source and destination logic (pages 10, 35, 45).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naum B. Levin whose telephone number is 571-272-1898. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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5/02/07

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PRIMARY PATENT EXAMINER